

(12)

EUROPEAN PATENT APPLICATION

(21) Application number: 80107628.2

(51) Int. Cl.³: G 09 G 3/28

(22) Date of filing: 04.12.80

(30) Priority: 08.01.80 US 110313

(43) Date of publication of application:
22.07.81 Bulletin 81/29

(64) Designated Contracting States:
BE CH DE FR GB IT LI NL SE

(71) Applicant: International Business Machines Corporation

Armonk, N.Y. 10504(US)

(72) Inventor: Kleen, Bergert G.
7 Laurel Street R.D. 5
Rolling Meadows Kingston New York(US)

(72) Inventor: Lamoureux, William R.
165 Highland Avenue
Kingston New York 12401(US)

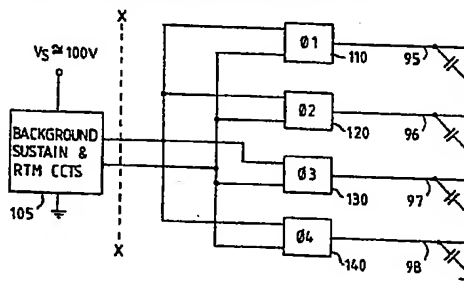
(72) Inventor: Martin, William J.
19 Parkside Drive
Lake Katrine New York 12449(US)

(74) Representative: Richards, John Peter
IBM UNITED KINGDOM PATENT OPERATIONS Hursley Park
Winchester Hants, SO21 2JN(GB)

(54) A method and circuit for producing avalanche currents in a gas discharge display panel.

(57) Large values of avalanche current are avoided in a gas discharge display panel by "staggering" in time the application of the sustain voltage waveforms to different portions of the display panel. A plurality of individual sustain circuit modules (110 to 140) each having two 100v FET's are connected to a common sustain circuit module (105) having another two 100v FET's. The staggered sustain operation is provided by selectively controlling the individual sustain circuit modules combine to alternatively produce 0-200v square wave or a 0-100-200v return-to-midpoint waveform by selectively controlling the FET's.

FIG. 5 BLOCK DIAGRAM OF A STAGGERED SYSTEM



EP 0 032 196 A2

- 1 -

A METHOD AND CIRCUIT FOR PRODUCING
AVALANCHE CURRENTS IN A GAS DISCHARGE DISPLAY PANEL

This invention relates to a method and circuit for producing avalanche currents in a gas discharge display panel.

Gas discharge display panels are provided with circuitry for producing a sustain voltage waveform which is applied to each of the discharge cells in the display panel. The sustain voltage causes selected panel areas to discharge due to current avalanche within the cell at a rate determined by the sustain voltage frequency. In this manner, the selected panel area has the appearance of being continuously illuminated..

Various problems are associated with driving large gas discharge display panels. On large displays, the gas avalanche current produced by the sustain voltages can become very large. These currents are drawn from a power supply to the display panel through parasitic inductances of the cabling and ground returns. The large avalanche current caused by the simultaneous sustain operation in each of the discharge cells produces a large time rate of change of current (di/dt) through these parasitic inductances to produce a voltage across the inductances. This voltage drop produces a "notching" and "ringing" of the voltage across the panel as illustrated in Figure 1. This degradation of the waveform will increase the minimum and decrease the maximum sustain voltages applied to the panel, thus reducing the operating margins. The large voltage drops and high frequency currents combine to produce electromagnetic interference and compatibility problems. Noise problems are caused by both conducted noise in the grounding systems and radiated noise from the cables.

One possible approach to eliminate these problems would be to divide some of the current paths among a plurality of independent sustain voltage circuits. The use of a plurality of independent

sustainers reduces notching to a certain extent but does not completely eliminate the problem. This technique also does not solve the conducted noise problems because it does not divide up the ground return paths. Another possible technique would be to design the panel itself to draw less avalanche current. Reducing the magnitude of the currents, however, also reduces the brightness and the operating margins of the panel.

It is therefore an object of the present invention to provide a new method and circuit for producing these avalanche currents which reduces the problem associated with parasitic inductances.

Accordingly, the invention provides a method for producing avalanche currents in a gas discharge display panel having a plurality of discharge cells, the method being characterised by:

providing a plurality of electrically isolated individual sustain circuit modules each responsive to a set of control signals to provide a respective sustain voltage waveform;

staggering in time the operation of the individual sustain circuit modules in response to the control signals whereby the sustain voltage waveforms are successively displaced from one another in time;

and applying each sustain voltage waveform to an associated different portion of the display panel whereby the avalanche currents periodically produced in the discharge cells of the display panel in response to the sustain voltage waveforms are similarly displaced in time to reduce voltage drops across parasitic impedances associated with the display panel.

- 3 -

An embodiment of the invention will now be described, by way of example, with reference to the accompanying drawings, wherein:-

Figure 1, previously referred to, compares an ideal sustain waveform with the waveform produced in a large display panel by conventional techniques;

Figure 2 illustrates a plurality of staggered sustain waveforms and the associated plurality of avalanche current spikes produced by the staggered sustain waveforms;

Figure 3 is a schematic illustration of a circuit for providing a bipolar 200 volt swing across a display panel discharge cell;

Figure 4 is a schematic illustration of a single-sided sustain unit which is used in the embodiment of the present invention;

Figure 5 is a schematic illustration of a multiple stagger sustain system in accordance with the present embodiment of the invention; and

Figure 6 is a timing diagram for the control of the FET's in the sustain circuit, the sustain voltage and discharge waveforms produced by the sustain circuit are being shown.

Figure 2 illustrates three staggered sustain waveforms applied to three different segments of a display panel. While three or four separate sustain drivers are described herein, the same technique may be used for any number of independent sustain drivers. The first segment is driven from zero voltage to a midpoint level of 100 volts for approximately three microseconds, and subsequently driven to a full voltage level of 200 volts where it remains for

- 4 -

approximately eight microseconds. The voltage returned to the midpoint voltage of 100 volts for three microseconds, and subsequently driven to zero potential for approximately eight microseconds. The second segment is driven in the same manner but the waveform is displaced in time from the first segment sustain waveform by approximately 100-500ns. The third segment is similarly driven by a sustain voltage by the same amount. This provides a staggered sustain waveform to the three segments of the display panel. In this manner, the avalanche current is staggered in time and consequently does not produce the large values of di/dt associated with conventional sustain waveform generators.

Sustain waveform generator circuits for large gas panel displays can be designed to use power MOS-FET's rather than bipolar transistors to thereby avoid the storage and gain problems associated with high voltage - high current bipolar transistors. The use of low cost power MOS-FET's would therefore reduce system hardware and operating costs. Unfortunately, 200 volt FET's are not readily available and have not been found to provide satisfactory operation in a sustain driver in accordance with the present technique.

Four 100 volt FET's in a bridge configuration as illustrated in Figure 3 can provide a 200 volt swing using a single 100 volt source. While FET's are shown in Figure 3, bipolar transistors can alternatively be employed as in the case of the IBM 240/480 Gas Panel. The voltage is alternatively delivered from one of FET's 10 or 20 to one of driver modules 30 or 35. One of the FET's 15 or 25 is provided to ground the other of the two driver modules 30 or 35 such that when FET 10 is biased "on" to provide source voltage to horizontal driver 30, FET 20 is biased "off" and FET 25 is biased "on" to place the vertical driver module 35 at ground.

- 5 -

potential. FET 15 must be biased "off" so that the horizontal axis can float to provide the required 100 volt potential between horizontal and vertical driver modules 30 and 35. The 200 volt voltage swing across panel cell 40 is accomplished by reversing the biases on FET's 10, 15, 20 and 25. While this technique will provide the proper voltage to sustain the cell discharge, it requires that both the horizontal and vertical axes float. This greatly increases the vertical data load time and thus the panel update time.

Figure 4 illustrates a 100 volt single-sided sustainer circuit which forms a part of the present embodiment and which of itself is described and claimed in our copending European Application (KI9-78-005). The circuit of Figure 4 is deemed "single-sided" since a 0-200 volt swing is produced at horizontal output line or axis 95, rather than alternatively applying 100 volts to either side of the panel cell 100 as in the Figure 3 arrangement. In this manner, the single-sided sustainer circuit provides the requisite 200 volt swing to sustain the cell discharge using 100 volt FET's, and allows the vertical axis to be tied to ground.

With reference to Figures 4 and 6, operation of the single-sided sustainer circuit will be described. Initially, at time T1, FET's 50 and 60 are biased "on", while FET's 45 and 55 are biased "off". The horizontal panel line 95 will be applied to ground through the horizontal driver module 80 and the sustain voltage as shown in Figure 6 will be applied to the panel cell to cause discharge of energized cell 100. Capacitor 90 is also charged to the source voltage through diode 65 and FET 50. At time T2, FET's 50 and 60 are biased "off" while FET 45 is biased "on" to thereby charge the line 95 to the source voltage through FET 45 and diode

- 6 -

75. The sustain voltage is then increased from the source voltage V_s to twice V_s by biasing FET 55 "on" at time T3. The voltage $2V_s$ is applied to the line 95 through FET's 45 and 55 and capacitor 90 which was previously charged to 100 volts. A positive discharge within energized cell 100 occurs at the 100 to 200 volt transition at time T3. At time T4, the sustain waveform is returned to the 100 volt level by first biasing "off" FET 45, then biasing "on" FET 50 to discharge the line 95 to the voltage across capacitor 90 (100 volts) through diode 70, capacitor 90, and FET 50. The process is repeated at time T5 by biasing FET 55 "off" and FET 60 "on" to produce the initial conditions as at time T1.

It may also be observed that the single-sided sustainer circuit of Figure 4 may be operated in a manner to provide a 200 volt peak-to-peak square wave without the return to 100 volt midpoint feature. This is accomplished by operating FET 55 at the same time as FET 45 such that both FET's 45 and 55 are biased "on" whenever FET's 50 and 60 are biased "off", and vice versa. Initially, with FET's 50 and 60 biased "on" and 45 and 55 biased "off", the horizontal line 95 will be pulled through the horizontal driver module to ground, and capacitor 90 will be charged to the source voltage, as described above. As FET's 50 and 60 are biased "off" and 45 and 55 are biased "on", the voltage $2V_s$ is applied to line 95 through FET's 45 and 55 and capacitor 90 which was previously charged to 100 volts. By repeating this process, a zero to 200 volt square wave is generated at line 95. Diodes 70 and 75 are not required for the zero to 200 volt square wave operation and can be omitted.

The single-sided sustainer circuit of Figure 4 readily lends itself to staggered sustain operation since the cell discharge occurs relative to transitions in FET's 55 and 60, while the transitions in FET's 45 and 50 do not determine the instant of discharge.

- 7 -

Referring to Figure 5, the circuit portion to the left of the dashed line X--X, designated the Background Sustain and Return to midpoint (RTM) circuit 105 corresponds to the circuit shown to the left of dashed line X--X of Figure 4. The circuit 105 is common to each of the remaining single-sided sustainer circuits 110-140, each of which comprise circuitry identical to that illustrated to the right of the dashed line X--X in Figure 4. The circuit of Figure 5 operates as follows. The FET's 45 and 50 contained in background sustain circuit 105 are operated as before as shown in Figure 6. Each pair of FET's in the sustainer modules 110-140 are operated in the same manner as FET's 55 and 60 of Figure 4. The turn on and turn off times of the latter FET's are however staggered to provide staggered waveforms to the respective horizontal lines 95-98. For example, if the FET's 60 and 55 respectively of sustainer module 110 are turned on at times T_1 and T_3 , as shown in Figure 6, to provide the discharges at times T_1 and T_3 via line 95, the corresponding FET's of sustainer module 120 are turned on at times $T_1 + \Delta T$, and $T_3 + \Delta T$, where ΔT is small compared to the period of the waveforms and represents the offset in time between sustain waveforms on lines 95 and 96. Sustainer modules 130 and 140 are likewise operated at intervals of ΔT so that all four waveforms are mutually staggered by ΔT . ΔT is, however, sufficiently small that all the waveforms are simultaneously at their maximum (200 volts) for part of the time during each period.

Thus, the single-sided sustainer allows a zero to 200 volt swing using only 100 volt FET's in a single-sided configuration, whereby the vertical axis may remain grounded. Only one transistor more per display unit is required than a system which uses 200 volt FET's inasmuch as the 200 volt design would require a separate return-to-midpoint transistor. Furthermore, the circuit requires

- 8 -

only a single high voltage power supply at 100 volts to produce the RTM waveform rather than the typical V_s and $2V_s$ power supplies regulated to $\pm 1\%$, as is conventionally done in RTM.

Additionally, due to the staggered sustain voltages, the peak currents in FET's 45 and 50 will not be much higher than the currents associated with the individual FET's 55 and 60. Since each of the sustainer modules 110-140 are electrically isolated from each other, the staggered sustain waveforms reduce the voltage drop across parasitic impedances as well as reducing electromagnetic interference, electromagnetic compatibility problems and noise problems associated with conducted and radiated noise.

CLAIMS

1. A method for producing avalanche currents in a gas discharge display panel having a plurality of discharge cells, the method being characterised by:

providing a plurality of electrically isolated individual sustain circuit modules (110, 120, 130, 140) each responsive to a set of control signals (A, B, C, D of Fig. 6) to provide a respective sustain voltage waveform;

staggering in time the operation of the individual sustain circuit modules in response to the control signals whereby the sustain voltage waveforms are successively displaced from one another in time;

and applying each sustain voltage waveform to an associated different portion of the display panel whereby the avalanche currents periodically produced in the discharge cells of the display panel in response to the sustain voltage waveforms are similarly displaced in time to reduce voltage drops across parasitic impedances associated with the display panel.

2. A circuit for performing the method claimed in claim 1, comprising:

a common first module having first and second switches each having an input, an output and a control terminal, the output of the first switch being connected to the input of the second switch and the output of the second switch being applied to ground, a

- 10 -

first diode connected at one end thereof to the input of the first switch and providing at the other end of the first diode a common output signal, the input of the second switch receiving a common input signal, and a voltage source applied to the input of the first switch; and

a plurality of electrically isolated individual second modules each for providing a respective sustain voltage waveform, each individual module having third and fourth switches each having an input, an output and a control terminal, the input of the third switch receiving the common output signal, the output of the third switch and the input of the fourth switch each being operatively connected to the display panel, and the output of the fourth switch providing the common input signal, and a capacitor connected at one end thereof to the input of the third switch and at the other end thereof to the output of the fourth switch;

whereby the connection to the display panel from the output of the third switch and the input of the fourth switch of each individual module provides a respective alternating waveform having a preselected frequency to a different portion of the display panel, the control signals being applied to the control terminals of the first, second third and fourth switches.

3. The circuit of claim 2, wherein substantially a zero voltage and a voltage of twice the source of voltage may be selectively produced at the display panel by each individual module under the selective control of the third and fourth switches associated with the individual module.

4. The circuit of claim 2, wherein each individual second module further comprises:

- 11 -

a second diode connected between the input of the third switch and the display panel, and a third diode connected between the output of the fourth switch and the display panel, whereby substantially a zero voltage, a voltage equal to the source voltage and a voltage twice the source voltage may be selectively produced at the display panel under the selective control of the third and fourth switches.

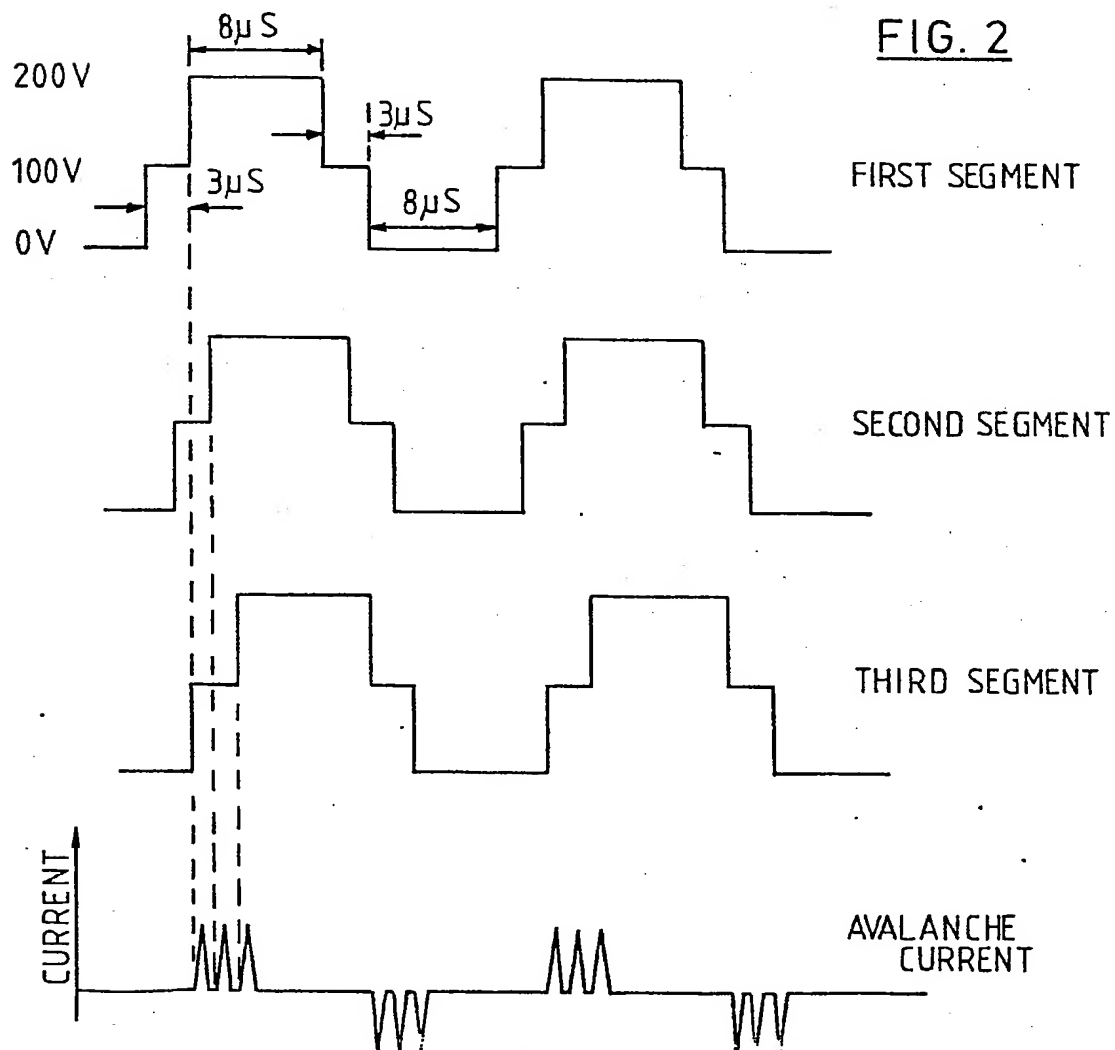
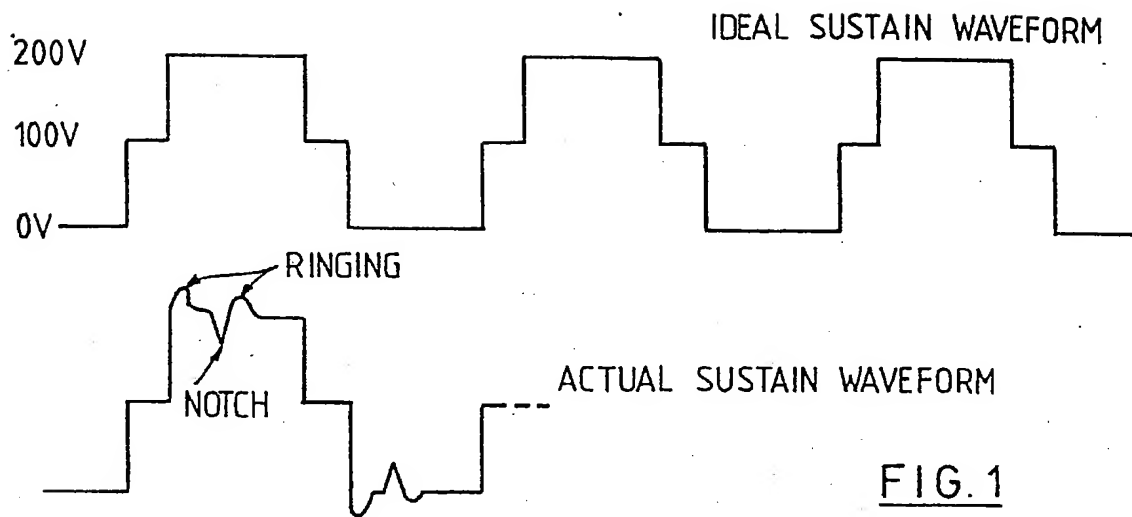
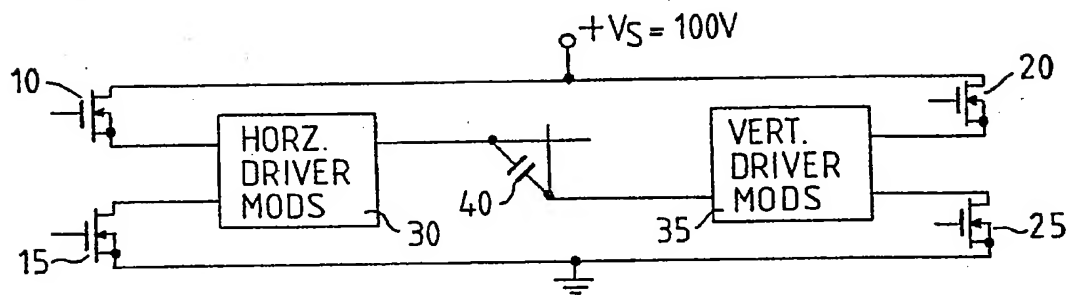
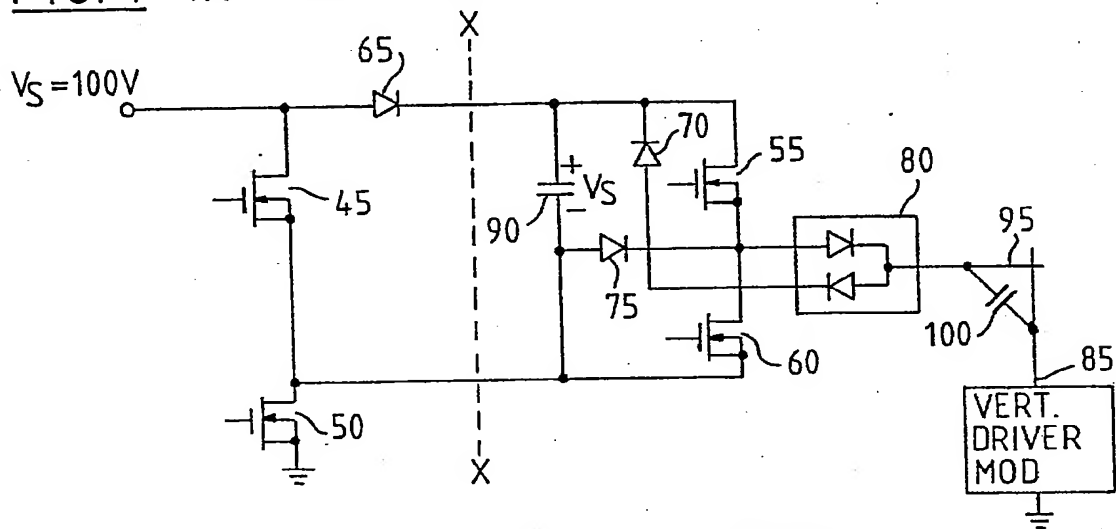
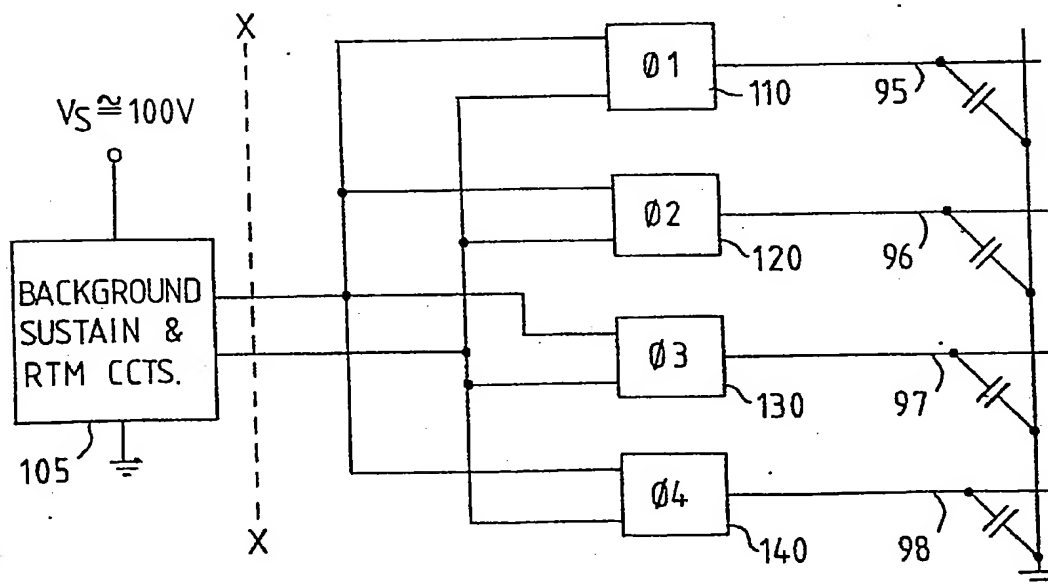
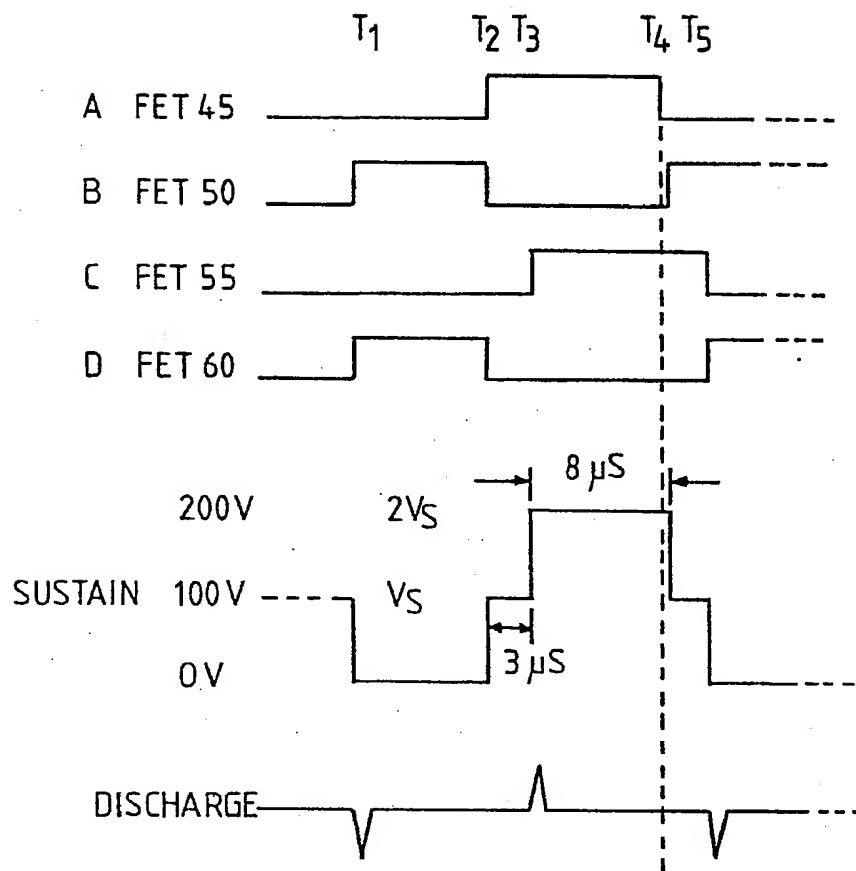


FIG. 3 BRIDGE SUSTAIN CONFIGURATIONFIG. 4 100V SINGLE SIDED SUSTAINFIG. 5 BLOCK DIAGRAM OF A STAGGERED SYSTEM

3/3

FIG. 6